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Der Präsident des Europäischen Patentamts;
Im Auftrag

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Le Président de l'Office européen des brevets
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Tracking picture tube

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Tracking picture tube

The invention relates to a drive circuit for driving a color display panel with display fields of display lines, to a display apparatus comprising such a drive circuit, and to a method of supplying drive signals to such a color display panel.

A tracking picture tube without a shadow mask is known from GB 2122415. Different phosphor strips extend in the horizontal direction and are arranged in groups. Each group comprises phosphors with the three primary colors red, green and blue. An electron beam is deflected by a deflection circuit. A system of electrodes is located adjacent to and in-between the phosphor strips. A deflection correction circuit measures the position of the electron beam with the electrodes and corrects the deflection of the electron beam to land on the centre of the correct one of the phosphor strips.

Usually, the input video signal to be displayed on the picture tube has an interlaced scan format wherein frames comprise successive fields of horizontal scanned lines which interlace each other in the vertical direction. Consequently, the groups of phosphor strips are interlaced scanned. In the fields in which the odd lines are present, the video signal is displayed on the phosphor strips of the odd numbered groups, and in the fields in which the even lines are present, the video signal is displayed on the phosphor strips of the even numbered groups.

However such an interlaced scan leads to strong artifacts such as: line flicker, line crawl, and resolution loss.

It is an object of the invention to decrease at least one of the artifacts caused by the interlaced scanning.

A first aspect of the invention provides a drive circuit for driving a color display panel with display fields of display lines as claimed in claim1. A second aspect of the invention provides a display apparatus comprising such a drive circuit as claimed in claim 7. A third aspect of the invention provides a method of supplying drive signals to such a color

display panel as claimed in claim 9. Advantageous embodiments are defined in the dependent claims.

The artifacts of interlaced scanning are known from known picture tubes with a shadow mask, but they are more visible in the tracking picture tube. The higher visibility is caused by the fact the lines are very sharply bounded in the vertical direction. The lines of known shadow mask picture tubes are smoothed by the size of the electron beam spot, which is typically larger than the vertical distance between the horizontally scanned lines. This smoothing will reduce at least the line flicker and the line crawl artifacts. Such a smoothing is impossible in a tracking picture tube.

The line flicker is caused by displaying different information shifted in time over a field period on successive groups of phosphor strips.

The resolution loss occurs when vertical motion with odd velocity (pixels/frame) is present. This resolution loss is also present in an interlaced input signal, and can only be repaired by de-interlacing processing. Therefore we will assume that the input signal is progressive, thus, the resolution loss is caused by the interlace display format, not by the input signal.

The line crawl typically occurs in image areas without detail (further referred to as flat areas). When the viewer tracks an object with vertical odd speed, the line structure becomes visible because the lines of two subsequent fields are seen at the same position (not 'interlaced'). This means that a flat area is no longer perceived as flat, but can be seen to consist of discrete lines. The line crawl is also visible if there is no motion in the image (e.g. in a full white image), because the viewer can still track a vertical odd speed over the screen. This is possible because at those speeds the line structure becomes visible. The lines seem to 'crawl' up or down. The line crawl causes an interlaced display to have restlessness, because any sudden eye movements cause the line structure to appear. This artifact can only be reduced by increasing the spot size in interlaced shadow mask picture tubes (the video processing has no effect in flat areas), or increasing the resolution (smaller line distance).

In the now following, the phosphor strips are more generally referred to as color display lines to indicate that the invention is not limited to picture tubes, but also is applicable to matrix displays such as poly-led displays. Even more general, the color display lines are referred to as pixel groups of color display elements. A pixel group comprises at least color display elements which have three primary colors, such that a group constitutes a full pixel which is able to provide white light. A group further might comprise, for example,

elements with another color, a white color and/or, a repetition of some but not all of the colors.

In the way of driving the color display lines as claimed in claim 1, in a display field, adjacent color display elements of the same pixel group do not all receive a display signal. The display elements which do not receive a display signal in a particular field will receive a display signal in another display field. Thus the total color produced by one pixel group is composed of contributions in different display fields of display elements of the pixel group having different colors. For example, if the display elements succeed each other in the field direction in the order red, green, blue, in a first display field only the red and blue display elements receive a display signal and the green display pixel does not contribute to the light produced by the pixel group, in a second display field only the green display pixel receives a display signal and the red and blue not.

In this way, smaller black areas (color display elements in a field period not receiving display signals) occur between the color display elements which receive display signals. Or said differently, the distance between color display elements generating light in a field period decreases with respect to interlaced scan wherein successively one pixel group of display elements does not receive display signals and thus does not produce light, while in the adjacent pixel group of display elements all elements receive display signals. Consequently, in the perception of the viewer, the amount of flicker decreases.

Many other structures of display elements are possible, the display elements of the same color may be arranged in a line, the display elements may be arranged in a delta-nabla structure. It is not required that all the display elements of the same group are provided with display signals in two consecutive display fields. For example, the blue display element may receive a signal in all display fields, the green display element only in odd numbered display fields, and the red display element only in half of the even numbered display fields. It is also possible that more than two display fields are required to supply display signals to all display elements of a pixel group.

The way of driving the color display elements in accordance with the invention differs from the known progressive scan wherein display signals are supplied to all color display elements of all pixel groups during each display field.

In the terminology used, a field or field period is defined as each display period wherein the display screen is scanned once (usually from top to bottom), but not all display lines have to be addressed. A frame is called a set of all the display lines, and consequently, a frame period is the time period required to address all the display lines once.

The frame period is typically equal to one progressive scanned or two interlace scanned field periods.

In an embodiment as defined in claim 2, the color display elements are arranged as color display lines, for example, phosphor display lines as used in a tracking picture tube. The adjacent phosphor display lines of a group, usually are horizontal lines which succeed each other in the vertical direction and which may emit red, green and blue light, respectively.

In an embodiment as defined in claim 3, although in each field period not all the color display lines of a group receive a display signal, in two successive field periods which form a frame period, all the display lines receive display signals. In this way the flicker is minimized because the maximum time elapsed between supplying the display signal to two adjacent color display lines of the same group is one field.

In an embodiment as defined in claim 4, which is referred to as color line interlace, in each display field, the black stripes are minimized to be a single color display line. The advantage is that the interlace artifacts are reduced.

The line flicker is reduced because a single white line in the progressive image is no longer only visible in one of the fields, but is partly displayed in each field. For example, green only is displayed in the odd fields, and red and blue are displayed in the even fields.

The line crawl is reduced, because the black area caused by color display lines to which no display signal is supplied and which occurs in-between the color display lines to which a display signal is displayed is much smaller than in the known interlaced scan. This makes the line structure less visible. In fact, the visibility of the line structure is largely determined by the green-green (line) distance, which has not changed, but the more evenly spread out intensity between the green lines (no large black area) make the line structure less visible, and therefore the line crawl (or restlessness) is also less.

The resolution loss is reduced, because in each group of the color display lines at least one receives a display signal, although in odd and even groups, different color display lines are activated.

In fact, the invention as claimed in claim 1, could be explained to be the known progressive scan of the display, wherein for each group of color display lines, at least one color display line will not receive a display signal and thus the corresponding color component of the corresponding video line is skipped. Such a skipping may easily be obtained by writing the video line(s) of the video signal into a memory as the three primary

color components representing the primary colors, and by reading the appropriate primary color component at the instant the video signal should be supplied to a color display line.

Any remaining artifacts, apart from the line crawl, may be reduced by processing the progressive image before the skipping of color display lines performed during the progressive-interlace conversion. The remaining line flicker can be reduced by reducing the bandwidth of the input video signal by a suitable vertical low-pass filter. This also holds for the known interlace format, but because in that case the line flicker is worse, the bandwidth must be further reduced than with the color line interlace format in accordance with an embodiment of the invention. Thus, the color line interlace format either produces less line flicker for the same resolution, or provides a higher resolution at the same amount of line flicker.

The artifacts of the known interlaced scanning are reduced without increasing the spot size of the picture tube, if used. Thus, unlike in picture tubes with a shadow mask, the interlace artifacts are reduced without reducing the sharpness.

In an embodiment as defined in claim 3, although not all the color display lines are progressive scanned, still, the visibility of flicker due to interlaced scanned color display lines decreases because not all the color display lines are interlaced scanned.

The embodiment as defined in claim 4 is based on the insight that the line flicker caused by an interlaced scan strongly increases with the brightness of the displayed information. Therefore, the line flicker caused by the low intensity blue color display lines which are interlace scanned is negligible, while the high intensity red and green color display lines have to be progressive scanned to prevent a visible flicker.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows a part of prior art tracking picture tube and the tracking mechanism,

Fig. 2 shows tracking electrodes and phosphor color display lines on the screen of the prior art tracking picture tube,

Fig. 3 shows a color display line scanning in accordance with an embodiment of the invention,

Fig. 4 shows another color display line scanning in accordance with an embodiment of the invention,

Fig. 5 shows a block diagram of a drive circuit for driving the tracking picture tube in accordance with an embodiment of the invention,

Fig. 6 shows a block diagram of a video processing circuit in accordance with an embodiment of the invention,

Fig. 7 shows a block diagram of a video processing circuit in accordance with an embodiment of the invention,

Figs. 8 shows a color line interlace display,

Fig. 9 shows a block diagram elucidating the line skipping, and

Figs. 10 show possible choices of addressing the color elements of the pixels for the delta-nabla arrangement of the color elements of the pixels.

Fig. 1 shows a part of the tracking picture tube and the tracking mechanism. The tracking picture tube 1 comprises: a portion of a screen 2 provided on its inside with phosphor strips and a neck portion 3 accommodating three electron guns 4 (schematically shown in the drawing) which each generate an electron beam 9. The phosphor strips extend in the horizontal direction and are arranged in groups of three strips, of which one group 5r, 5g, 5b is shown in Fig. 1. The group 5r, 5g, 5b emits the primary colors red R, green G, and blue B, respectively, when hit by the electron beam 9 emitted by the guns 4. The three strips 5r, 5g, 5b are arranged in a regular alternating order such that two strips representing the same color always are separated by two strips representing the other colors.

A deflection unit 10 is arranged between the electron guns 4 and the screen 2 to deflect the beams 9 towards the correct position 7 on the correct one of the phosphor strips 5r, 5g, 5b. The beam 9 of a particular gun 4 is usually deflected towards phosphor strips 5r, 5g, 5b with the same one of the primary colors R, G, B. This is why the guns 4 are usually referred to as the red gun, the green gun and the blue gun.

Of course a different number of guns 4 might be used in the picture tube 1 in any different combination of colors of the phosphor strips 5r, 5g, 5b. For example, two green guns, one red gun and one blue gun may be used.

The screen 2 is provided with two comb-shaped conducting tracking electrodes 12 and 13, and the correct tracking of the electron beams 9 is sensed and controlled electrically. In the case of optical tracking, light emitting strips similar to the

phosphor strips 5r, 5g, 5b may be used as tracking electrodes 12 and 13, and the light emitted from these strips is detected by light sensors.

Each electrode 12, 13 has a number of finger portions 14, 15 which are arranged in an interleaved manner. The electrodes 12, 13 may be formed on the screen 2 using lithography. In Fig. 1, only one pair of respectively interconnected electrodes 12, 13 is provided, however, it is possible to interconnect the electrodes 12, 13 in groups.

An electron beam 9 hitting the centre of one of the phosphor strips 5r, 5g, 5b causes the same amount of electric charge to flow to the finger portions 14, 15 adjacent to one of the strips 5r, 5g, 5b. Any deviation from the centre of one of the strips 5r, 5g, 5b will be detected as a potential difference by a comparator 17. The output 18 of the comparator 17 thus indicates the position of the beams 9 with respect to the strips 5r, 5g, 5b. The tracking processing circuit 19 processes the output signal available at the output 18 to drive the deflection unit 10 such that the beam 9 deflection is influenced to keep the beam 9 at the centre of the strips 5r, 5g, 5b during scanning of the beam 9 along the strips 5r, 5g, 5b across the screen 2.

As the invention is not limited to a tracking picture tube, the strips 5r, 5g, 5b are more generally referred to as color display lines r, g, b (see Fig. 2). And a set of three successive strips comprising all the primary colors R, G, B is more generally referred to as a group GR1, GR2, ... of color display lines r, g, b.

Fig. 2 shows the tracking electrodes and the phosphor color display lines on the screen of the tracking picture tube.

The phosphor strips PR, PG, PB which are referred to as the color display lines r, g, b are arranged between the finger portions 14 and 15 of the tracking electrodes 12 and 13. The phosphor strips PR, PG, PB emit the primary colors R, G, B, respectively. The color display lines r, g, b are grouped in groups GR1, GR2, GR3, ...

In the known progressive addressing of a tracking picture tube, in a display field period TF1, TF2, ..., (see Fig. 3) each line in an input video signal VI is mapped to a corresponding display line TL1, TL2, ... of three neighboring phosphor stripes PR, PG, PB on the display panel 1. The number of lines in the input video signal VI should be equal to the number of display lines TL1, TL2, ... If this number differs, known video processing algorithms such as de-interlacing, spatial scaling and frame rate conversion should be applied to convert a video signal VI that does not have this progressive scan format to the same number of video lines as the display lines TL1, TL2, ... of the display panel 1.

To reduce the required addressing rate (line deflection frequency in the tracking picture tube), it is known to apply interlace addressing (or scanning). In an interlaced addressed display, each full frame is divided into two fields, one consisting of the odd, and the other of the even display lines TL1, TL2, ... The display of the input video signal VI which is an interlaced signal with a same number of video lines as the display lines TL1, TL2, ..., is straightforward. If the number differs, known frame rate converters should convert the input video signal to have the same number.

However, the interlaced addressing scheme gives rise to artifacts. The artifacts are known from traditional picture tubes with a shadow mask, but they are more visible in the tracking picture tube or a matrix display. The higher visibility is caused by the fact the display lines TL1, TL2, ... are very sharply bounded in the vertical direction. The display lines of traditional shadow mask picture tubes are smoothed by the size of the electron beam spot, which is typically larger than the vertical distance between the horizontally scanned lines. This smoothing will reduce at least the first two mentioned artifacts. Such a smoothing is impossible in a tracking picture tube or a matrix display.

The line flicker is caused by displaying different information shifted in time over a frame period TF1, TF2, ... on successive groups GR1, GR2, GR3, ... of phosphor strips PR, PG, PB.

The resolution loss occurs when vertical motion with odd velocity (pixels/frame) is present. This resolution loss is also present in an interlaced input video signal VI, and can only be repaired by de-interlacing processing. Therefore we will assume that the input signal VI is progressive, thus, the resolution loss is caused by the interlace display format, not by the input signal VI.

The line crawl typically occurs in image areas without detail (further referred to as flat areas). When the viewer tracks an object with vertical odd speed, the line structure becomes visible because the display lines TL1, TL2, ... of two subsequent fields TF1, TF2, ... are seen at the same position (not 'interlaced'). This means that a flat area is no longer flat, but can be seen to consist of discrete display lines TL1, TL2, ... The line crawl is also visible if there is no motion in the image (e.g. in a full white image), because the viewer can still track a vertical odd speed over the screen 2. This is possible because at those speeds the line structure becomes visible. The display lines TL1, TL2, ... seem to 'crawl' up or down. The line crawl causes an interlaced display to have restlessness because any sudden eye movement may cause the line structure to become visible. This artifact can only be reduced

by increasing the spot size in interlaced shadow mask picture tubes (the video processing has no effect in flat areas), or increasing the resolution (smaller line distance).

The addressing scheme in accordance with embodiments of the invention will be elucidated with respect to the following Figs..

Figs. 3 and 4 show a color display line scanning in accordance with different embodiments of the invention. In both Figs., in vertical direction the groups GR1, GR2, GR3, ... , GRn of color display lines r, g, b are shown for a display field period TF1, TF2, ... Each group GR1, GR2, GR3, ... , GRn corresponds to a display line TL1, TL2, ... of video information VI to be displayed. The crosses indicate for each display field period TF1, TF2, ... which color display lines r, g, b are addressed to display information. A display signal VD is supplied to the color display lines r, g, b indicated by a cross, and no display information VD is supplied to the color display lines r, g, b not indicated by a cross. Thus, each column of crosses indicates which color display lines r, g, b in the corresponding display field period TF1, TF2, ... are addressed, the other, non-addressed color display lines r, g, b are skipped.

Fig. 3 shows that in each of the display field periods TF1, TF2, ..., only half the number of color display lines r, g, b is addressed, wherein each addressed color display line r, g, b is succeeded by a non-addressed color display line r, g, b. The position of the addressed and non-addressed color display lines r, g, b in successive display field periods TF1, TF2, ... interleaves such that all color display lines r, g, b are addressed in successive display field periods TF1, TF2, ... This driving scheme of the display device is referred to as color line interlace because the color display lines r, g, b are displayed in an interlaced manner. In the known interlaced scanning scheme, the groups GR1, ..., GRn of the color display lines TL1, TL2, ... are interleaved addressed in successive fields.

The advantage of using this color line interlace format, is that the interlace artifacts are reduced.

The line flicker is reduced, because a single white line in the progressive input image VI is no longer only visible in one of the display fields TF1, TF2, ..., but is partly displayed in each display field TF1, TF2, ... (for example, green in one and red and blue in the other display field).

The line crawl is reduced, because the black area in-between the color display lines r, g, b is much smaller than the three color display lines r, g, b in the known interlaced scanning scheme, and thus the line structure will become less visible. In fact, as an example, in today's tracking tubes, the visibility of the line structure is largely determined by the distance between the high luminance green-green color display lines g. In the drive schemes

in accordance with the embodiments of the invention, this distance has not changed. But, the more evenly spread out intensity between the green color display lines g (no large black area) causes the line structure to become less visible, and therefore the line crawl (or restlessness) will also decrease.

The resolution loss is reduced because all the video lines in the progressive input image VI are represented in each field TF1, TF2, ..., although only for a subset of the colors R, G, B and consequently odd and even lines have a different color.

Any remaining artifacts, apart from the line crawl, may be reduced by processing the progressive input image VI before discarding the not needed video lines in the progressive-interlace conversion in accordance with the invention. Thus, remaining line flicker can be reduced by reducing the bandwidth of the progressive input image VI by a suitable vertical low-pass filter. This also holds for the known interlace format, but because in that case the line flicker is worse, the bandwidth must be further reduced than with the color line interlace format in accordance with an embodiment of the invention. Thus, the color line interlace either has less line flicker for the same resolution, or more resolution at the same amount of line flicker.

The interlace artifacts are reduced without increasing the spot size, so unlike in traditional picture tubes, the interlace artifacts are reduced without reducing the sharpness.

Fig. 4 shows again a driving scheme of the display device in which in each field only half of the color display lines r, g, b is addressed, wherein all the color display lines are addressed in two consecutive display field periods TF1, TF2, ...

In the odd display field periods TF1, TF3, ... the color display lines r are addressed in every group GR1, GR2, ... , GRn (or line TL1, TL2, ...). In the even display field periods TF2, TF4, ... the color display lines g are addressed in every group GR1, GR2, GR3, ... , GRn (or line TL1, TL2, ...). Thus, the red and green color display lines r and g are progressive scanned in alternating display field periods TF1, TF2, ...

The blue color display lines b are interlaced scanned. In the even display field periods TF2, TF4, ..., the color display lines b are addressed in the odd lines TL1, TL3, ... In the odd display field periods TF1, TF3, ..., the color display lines b are addressed in the even lines TL2, TL4, ...

In all embodiments, the basic idea is to decrease the distance between addressed color display lines r, g, b with respect to the known interlaced scanning wherein the groups GR1, GR2, GR3, ... , GRn are addressed (or scanned) interlaced. The decreased

distance between addressed color display lines r, g, b in a particular display field period TF1, TF2, ... which produce light decreases the artifacts of the interlaced group addressing.

The basic processing to map the input signal VI to the scanning format elucidated with respect to Fig. 4, is the same as in the color line interlace scheme as elucidated with respect to Fig. 3. Starting from a (suitably pre-processed) progressive input video signal VI, we have to discard the video lines that are not addressed. In each display field TF1, TF2, ... again only half of the display lines TL1, TL2, ...are used to display information.

In the embodiment of Fig. 4, the line crawl is completely removed, because the two colors that contribute most to the (high resolution) luminance, red R and green G, are no longer interlaced displayed. This means that, whatever the speed of motion (tracking) on the display screen 2, no line structure will become visible. As a consequence, also the resolution loss is strongly reduced (the information of each video line is present in each field TF1, TF2,... , in red R or in green G, even with critical velocities).

A disadvantage of this driving scheme is that, at a 50Hz field rate, a 25Hz (color) large area flicker component (but no line flicker) will occur. Even though the combination of progressive scan of red R and green G, and interlaced scan of blue G (other combinations are also possible) is the one with the least luminance flicker, it may still be visible at 50Hz field rate. Therefore, it is advantageous to increase the field rate, for example to 100 Hz to render this flicker invisible.

A typical artifact arising from color sequential display is color break up. This is either caused by incorrect motion rendering (frame repetition), or by sudden eye movements. The first cause is not present if we make sure that each original frame is correctly converted to the higher frame rate, i.e. with motion compensation. The second cause is harder to overcome, and might demand higher frame rates.

Fig. 5 shows a block diagram of a drive circuit for driving the tracking picture tube. A video processing circuit 102 receives an input video signal VI and a control signal CS1, and supplies display signals VD to the display panel 101. An addressing circuit 103 receives a control signal CS2 and an optional feedback signal DFB to supply addressing signals DS to the display panel 101. A control circuit 104 receives synchronization information SY and supplies the control signals CS1 and CS2.

If the display panel 101 is a tracking picture tube 101, the addressing circuit 103 is a deflection circuit which generates deflection signals DS to deflect one or more electron beam(s) 9 in the tracking picture tube 1 by means of deflection unit 10 to scan

(address) fields (the display fields TF1, TF2, ...) of lines (the display lines TL1, TL2, ... which comprise the color display lines r, g, b which are the phosphor strips PR, PG, PB). The feedback signal DFB provides a signal indicating the beam position with respect to the phosphor strips PR, PG, PB. The deflection circuit adapts the deflection signals DS to position the electron beam(s) 9 by means of the deflection unit 10 on the centre of the phosphor strips PR, PG, PB.

If the display panel 101 is a matrix display 101, the addressing circuit 103 comprises a select driver (usually the row driver) to address lines of pixels. The feedback signal DFB is not required. The video processing circuit 102 supplies display signal VD via a data driver (usually the column driver) to the display panel 101.

The control circuit 104 receives the synchronization information SY of, or belonging to, the video information VI and supplies horizontal and vertical position information CS2 to the addressing circuit 103 to lock the addressing of the display panel 101 to the video information VI, or the other way around. In the last case, the video processing circuit 102 has to resample, and if required to scale, the video information VI to fit the resolution of the display panel 101. The resampling and scaling can be done in any known manner.

The known video processing circuit 102 suitable to progressive scan the groups GR1, GR2, GR3, ... , GRn or lines TL1, TL2, ... has to be adapted to skip color display lines r, g, b. The color display lines r, g, b which should not display information (see Figs. 3 and 4) can be easily skipped by not supplying display signals VD to these lines TL1, TL2, ... It is even possible to lower the addressing rate as only half of the color display lines r, g, b have to be addressed in each display field TF1, TF2, ... Consequently, the drive schemes in accordance with embodiments of the invention do not require the high addressing rate of the known progressive scan addressing scheme and provide less artifacts than the known interlaced scan addressing scheme wherein complete lines TL1, TL2, ... are skipped.

Fig. 6 shows a block diagram of a video processing circuit in accordance with an embodiment of the invention. The video processing circuit 102 comprises a discard circuit 21 for skipping color display lines r, g, b in the input video signal VI which has a progressive addressing format. If the input signal VI is an interlaced signal, a known de-interlacer 20 is added to convert the interlaced input signal VI into a progressive signal before skipping the video signal for color display lines r, g, b which should not be addressed.

The video processing circuit 102 may further comprise a known pre-processing block (not shown) which performs the pre-processing for the progressive

addressing scheme of the input video signal VI to one of the addressing schemes in accordance with an embodiment of the invention. The pre-processing may comprise a bandwidth reduction, a spatial scaling, a frame rate conversion or correction for the different spatial positions of the phosphor lines.

Fig. 7 shows a block diagram of a video processing circuit in accordance with an embodiment of the invention.

A number of different situations can be distinguished depending on the input or source format of the input display signal VI and the driving or addressing format. The source formats (assume that each input line contains a R, G and B signal) are interlace or progressive video. The addressing formats of the display 1 are: the known interlace, color line interlace (Fig. 3) and mixed color sequential (Fig. 4).

Fig. 7 shows the basic signal flow from each of the inputs formats to each of the addressing formats. The input formats are indicated by PRO for the progressive format and by INT for the interlaced format. The drive formats are indicated by PRD for the progressive format and by IND for the interlaced format. If the source and driving format have a corresponding format, no processing is necessary. However, if the source and driving format are different, a conversion is necessary.

It is assumed that the source and driving format have the same number of lines (in each frame). If the source and display format have a different number of lines, the signal is scaled first.

A de-interlacer DI is provided if the interlaced source format INT has to be processed into a progressive display format PRD. If the progressive source format PRO has to be transformed into an interlaced display format IND, the progressive source format is processed by a progressive to interlace converter PI. The switching functions S1 and S2 symbolically indicate that, depending on the conversion required, either the de-interlacer DI or the progressive to interlace converter PI is active. It is also possible that both the de-interlacer DI and the progressive to interlace converter PI is active.

The simplest situation arises if the input and driving format have equal number of lines for each color per field. For example, an interlace input (N lines per frame, ½N lines per field) can be connected directly to the display in case of the known interlace driving format, each line (group of RGB) of the input can be written to the display directly.

Also the color line interlace display (Fig. 3) can be driven without video processing from an interlace source because the signals correspond in number and color.

However, it will depend on the details of the addressing where each input line is written on the screen. This is elucidated with respect to Fig. 8.

If the source format is a progressive signal PRO, or if an interlace source format INT is converted to a progressive format by the de-interlacer DI, the possibility exist to either display the image in the progressive display format PRD, or convert the output of the de-interlacer DI back to an interlace display format IND which saves bandwidth. The progressive to interlace converter PI picks those lines from the input signal that have to be displayed on the display, as was explained with respect to Figs. 3 and 4. It will now depend on the driving format required (color line interlace or mixed color sequential or any other subset of the color lines) how the conversion should work. For example, if the driving format is color line interlace (see Fig. 3), and if the input lines are numbered n=1,2..N, and k is an integer number, the conversion should work as follows:

in odd fields TF:

for n=2k: pass R,B, discard G

for n=2k+1 discard R,B, pass G

in even fields TF:

for n=2k: pass G, discard R,B

for n=2k+1: discard G, pass R,B

This conversion is further elucidated with respect to Fig. 9.

Figs. 8 shows a color line interlace display.

The three colors R, G, B of each input line are displayed on the display screen in the color line interlace format (Fig. 3). In principle the addressing is the same as for the known interlaced display, but the input lines are written on different color lines r, g, b on the screen.

Fig. 8A shows that the blue line from the input line is written in the center, while in Fig. 8B, the green line from the input line is written in the center. Thus, although the interlace format shown in Figs. 8 is almost identical, a single line delay can convert the two situations into each other. In both Fig. 8A and 8B, two successive fields TF1 and TF2 are shown. In each one of the fields TF1 and TF2, the color lines r, g, b are addressed interleaved, wherein the color lines r, g, b which are addressed in the one field TF1 are not addressed in the other field TF2, and the other way around.

Fig. 9 shows a block diagram elucidating the line skipping.

The input signals R, G, B are passed or skipped with the switches SR, SG, SB, respectively. The switches SR, SG, SB are set to 1 (pass) for R, B and 0 (discard) for G in the

shown line (e.g. line 2k in an odd field). The switches SR, SG, SB alter position after each line and between fields. For the Fig. 8A situation, the delays required to have the correct signal available at the correct instant are provided as the line delays LDR and LDB for R and B, respectively.

For other driving formats in accordance with embodiments of the invention, a similar selection (progressive to interlace conversion) scheme is possible. For example, the mixed RG-color-sequential, B-interlace format (see Fig. 4), will switch as follows:
In odd fields: R always 1, G always 0, and B 1 for the lines n=2k and 0 for n=2k+1.
In even fields: R always 0, G always 1, and B 1 for the lines n=2k+1 and 0 for n=2k.

Note that it is not possible to make use of the direct interlace source to interlace display connection, because the number of lines of each color is not the same. Therefore, the combination of consecutive color lines into one 'normal' line is not possible, it depends on the actual scanning of the display (the colors 'expected' by the display), which lines must be combined after selection.

The general principle of color interlaced display, wherein not all light emitting elements of a pixel group GR receive a display signal in each field is also applicable to other structures than pixels which are arranged in lines in the display. It is relevant that out of a pixel group of R,G and B (pixel) elements, a subset (not all) is addressed in each field, such that all subsets together form the whole frame. A group of exactly one R,G and B is commonly denoted as a pixel or a full color pixel. However the full color pixel may comprise a further color element. For example, the pixel groups may be arranged in a 'delta-nabla' structure, or similar patterns such as stripes, bayer, pentile.

To obtain as few artifacts as possible by only using half of the light generating elements on the screen during each field, the remaining structure in each individual field should be as invisible, or unstructured, as possible. Many degrees of freedom exist in selecting which elements should be addressed in which field because it is possible to choose from many subsets of color elements which should in a particular field be addressed. These subsets may differ for each color and for each field.

Figs. 10 show possible choices of addressing the color elements of the pixels for the delta-nabla arrangement of the color elements of the pixels.

Fig. 10A shows the delta-nabla structure of the color elements R, G, B in the pixels GR1, GR2, ... Figs. 10B to 10E show possible addressing schemes for the blue color elements B in a sequence of two fields which form one frame wherein all color elements R, G, B are addressed. The crossed squares indicate the blue color elements B which are

addressed in a first one of the fields (for example, the odd fields), and the white squares indicate the blue color elements B which are addressed in the second one of the fields (for example, the even fields).

If the color elements of each color are considered independently (no mixed color-sequential formats), there are, as shown in Figs. 10B to 10 E, at least four different good ways to address half of the pixels in each field. For each of the color elements R, G and B, one of the four different addressing possibilities may be selected. For example, the selections may be: all color elements R, G, B are addressed in accordance with Fig. 10D, or all color elements R, G, B are addressed in accordance with Fig. 10B, or the red color elements R are addressed in accordance with Fig. 10D, the green color elements G are addressed in accordance with the inverse scheme (crossed and non-crossed squares are interchanged) of Fig. 10D, and the blue color elements B are addressed in accordance with Fig. 10C, or both the red R and blue B color elements are addressed in accordance with Fig. 10C and the green color elements G are addressed in accordance with Fig. 10E, or the red R and blue B color elements are addressed in accordance with Fig.10D and the green color elements are addressed in accordance with Fig. 10D.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims.

For example, Figs. 3 and 4 show embodiments in accordance with the invention, only. It is possible to apply the basic idea of decreasing the distance between addressed color display lines r, g, b with respect to the known interlaced scanning wherein the groups GR1, GR2, GR3, ... , GRn are addressed or scanned interlaced to a display which has more than three color display lines r, g, b in the groups GR1, GR2, GR3, ... , GRn.

It is also possible to apply the interlaced scan shown in Fig. 4 for the color display line b on another color, or on two colors.

The addressing of the display 1 in accordance with an embodiment of the invention does not require specific video processing. As long as each color R, G, B addressed on the display 1 in a particular field TF1, TF2, ... is provided with a signal VD (obviously the signal must correspond to the color R, G, B of the phosphor line r, g, b), the addressing scheme will function.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The invention can be implemented by

means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A drive circuit for driving a color display panel with display fields of display lines, the color display panel comprising pixel groups forming a repetitive pattern of adjacent color display elements, each one of the pixel groups comprising a smallest set of adjacent color display elements within the repetitive pattern, the smallest set comprising at least three color display elements, the drive circuit comprising:

an addressing circuit for addressing said color display elements in the display fields,

a video processor for converting an input video signal into display signals being supplied to said color display elements, and

a controller for controlling the video processor and the addressing circuit to supply the display signals to at least one of the pixel groups:

in a first one of the display fields to at least one of the color display elements, but not to all different color display elements of the at least one of the pixel groups, and

in a second one of the display fields to at least one of the color display elements, but not all different color display elements of the at least one of the pixel groups, wherein in a sequence of successive display fields all color display elements receive display signals and wherein in at least one display field of the sequence at least two color display elements of the at least one of the pixel groups receive display signals.

2. A drive circuit as claimed in claim 1, characterized in that the color display elements are color display lines.

3. A drive circuit as claimed in claim 2, characterized in that the second display field period immediately succeeds the first display field period and that in the successive first and second display fields, which form a display frame, all color display lines receive display signals.

4. A drive circuit as claimed in claim 2, characterized in that the controller is adapted for controlling the video processor and the addressing circuit to supply the display

signals to the color display lines of the pixel groups either in the first display field period or in the second display field period, while in a display field one of two color display lines of a same color in two adjacent pixel groups does not receive display signals.

5. A drive circuit as claimed in claim 2, characterized in that the controller is adapted for controlling the video processor and the addressing circuit to supply the display signals in the first and the second ones of the display fields to obtain an interlace display of a first set of the color display lines and a progressive display of a second set of the color display lines.

6. A drive circuit as claimed in claim 5, characterized in that the first set of color display lines comprises the color display lines being blue, the first set of color display lines being interlaced displayed with P fields per second and L lines per field, while the second set of color display lines comprises the color display lines being red and green, the second set of color display lines being progressive displayed with P/2 fields per second and 2*L lines per field.

7. A display apparatus comprising a drive circuit as claimed in claim 1.

8. A display apparatus as claimed in claim 7, characterized in that the display apparatus comprises a tracking display tube, wherein the color display elements are color display lines formed by phosphor stripes.

9. A method of supplying drive signals to a color display panel with display fields of display lines, the color display panel comprising pixel groups forming a repetitive pattern of adjacent color display elements, each one of the pixel groups comprising a smallest set of adjacent color display elements within the repetitive pattern, the smallest set comprising at least three color display elements, the method comprising:

addressing the color display elements in the display fields;

converting an input video signal into display signals to be supplied to the color display elements; and

controlling the video processor and the addressing circuit to supply the display signals to at least one of the pixel groups:

in a first one of the display fields to at least one of the color display elements, but not to all different color display elements of the at least one of the pixel groups, and

in a second one of the display fields to at least one of the color display elements, but not all different color display elements of the at least one of the pixel groups, wherein in a sequence of successive display fields all color display elements receive display signals and wherein in at least one display field of the sequence at least two color display elements of the at least one of the pixel groups receive display signals.

ABSTRACT:

A method of supplying drive signals to a color display panel (1;101) with display fields (TF1; TF2; ...) of display lines. The panel (1;101) comprises successive pixel groups (GR1; GR2; ...) of color display elements (r, g, b), representing at least all three primary colors (R, G, B). The color display elements (r, g, b) are addressed (3) in a display field (TF1; TF2; ...) to receive display signals (VD). In a first display field (TF1) the display signals (VD) for at least one of the pixel groups (GR1; GR2; ...) are supplied to at least one, but not to all, of the color display lines (r, g, b) of the at least one of the pixel group (GR1; GR2; ...). In a second display field period (TF2) the display signals (VD) are supplied to at least one, but not to all, of the color display lines (r, g, b) of the at least one of the pixel group (GR1; GR2; ...). In a sequence of successive display fields (TF1; TF2; ...) all color display elements (r, g, b) receive display signals (VD). In at least one display field (TF1; TF2; ...) of the sequence at least two color display elements (r, g, b) of the at least one of the pixel groups (GR1, GR2, ...) receive display signals (VD).

(Fig. 5)

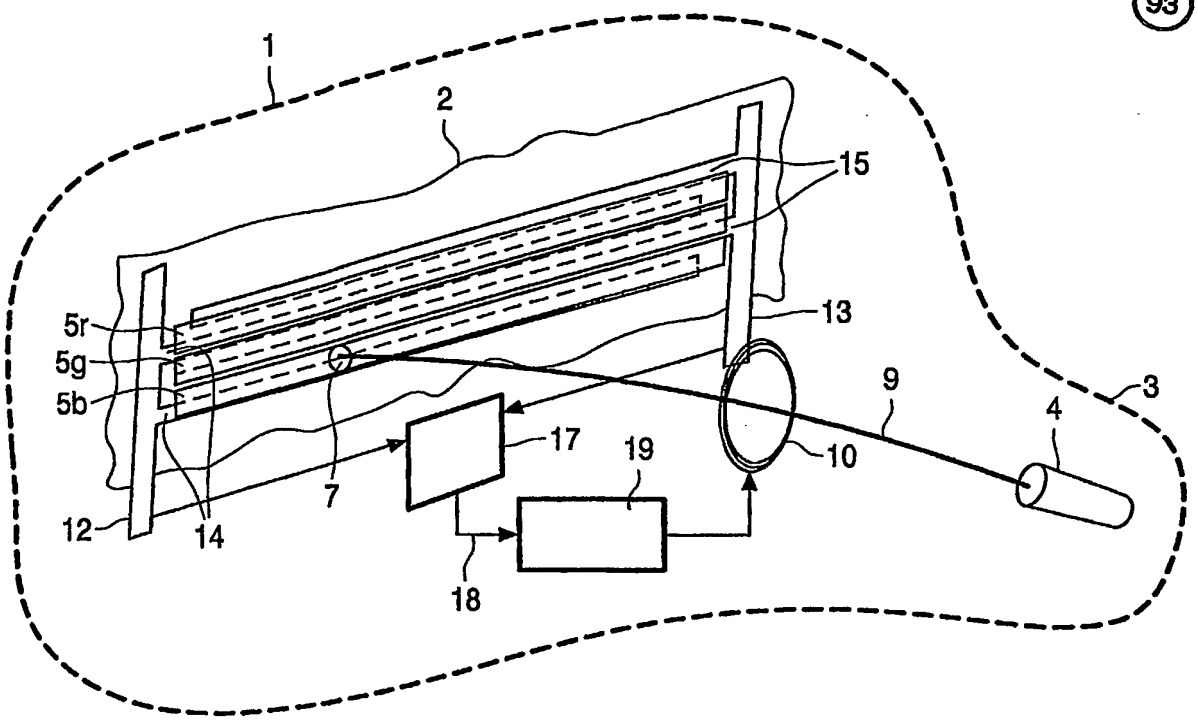
1
2
15
5r
5g
5b
13
9
3
4
17
19
10
7
12
14
18

FIG. 1

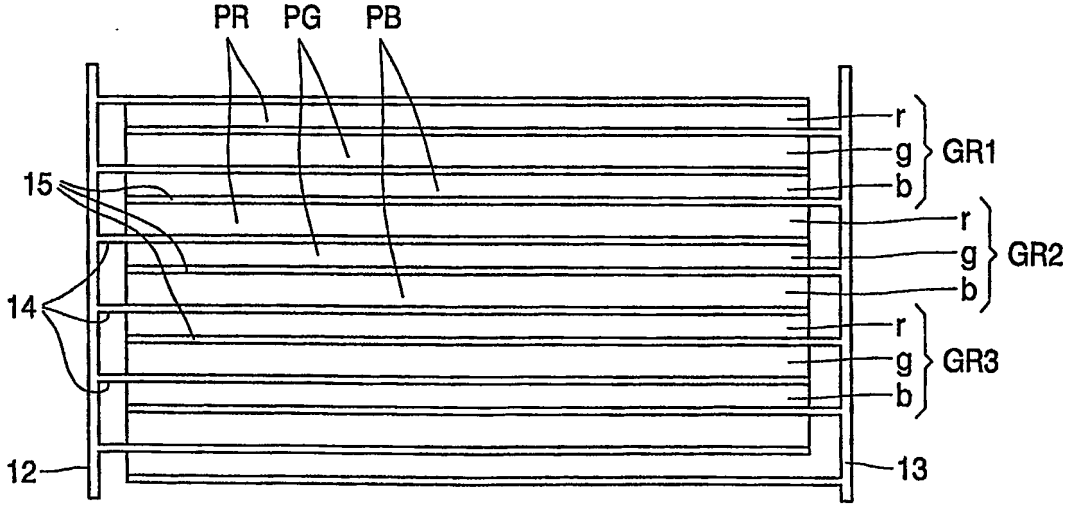
PR
PG
PB
r
g
b
GR1
GR2
GR3
15
14
12
13

FIG. 2

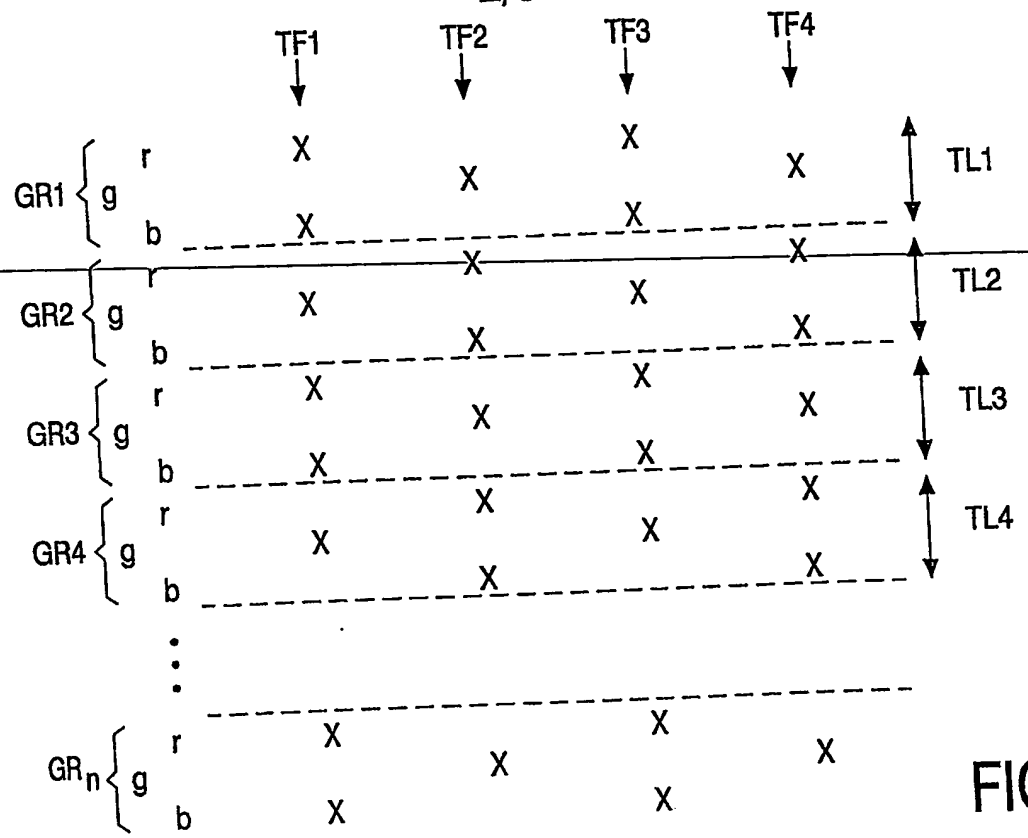
TF1
TF2
TF3
TF4
GR1
GR2
GR3
GR4
GRn
r
g
b
TL1
TL2
TL3
TL4

FIG. 3

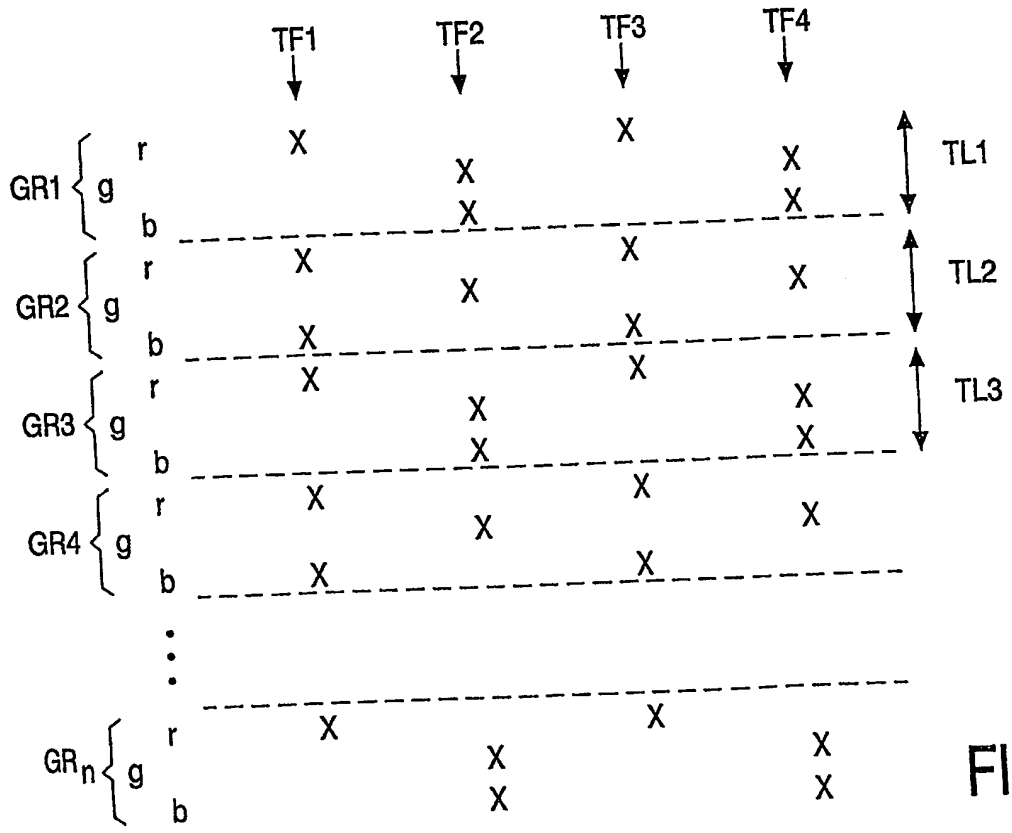
TF1
TF2
TF3
TF4
GR1
GR2
GR3
GR4
GRn
r
g
b
TL1
TL2
TL3

FIG. 4

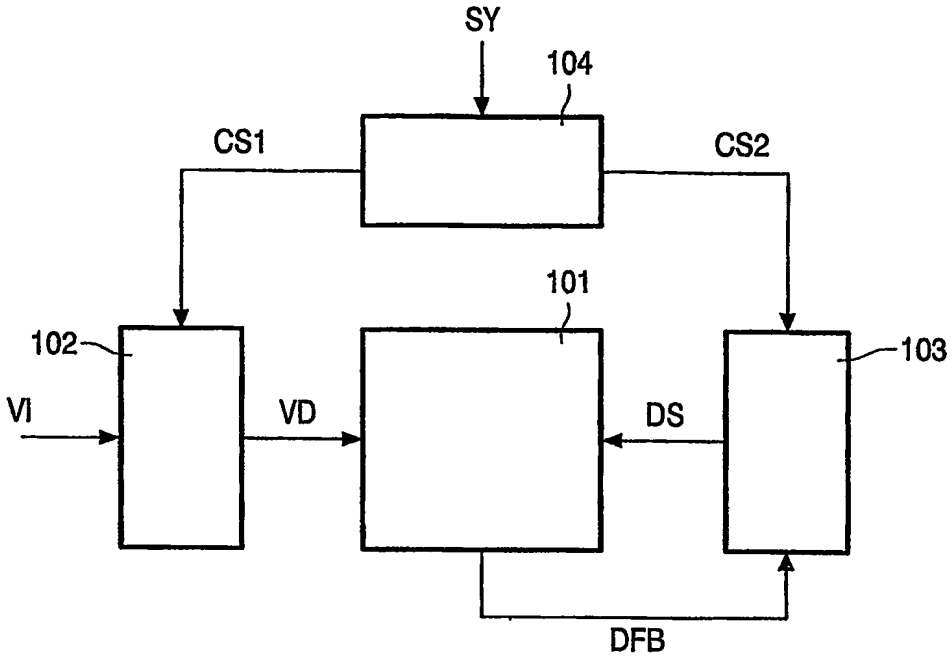

FIG. 5

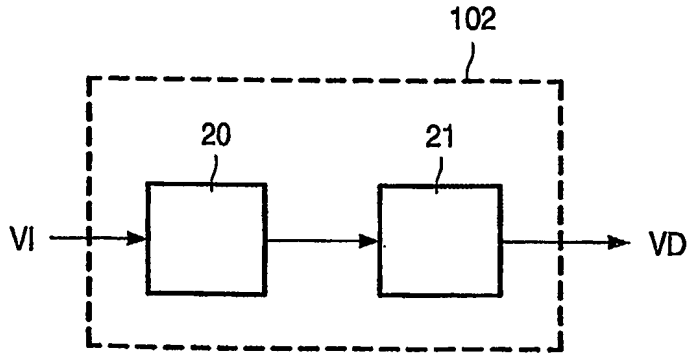

FIG. 6

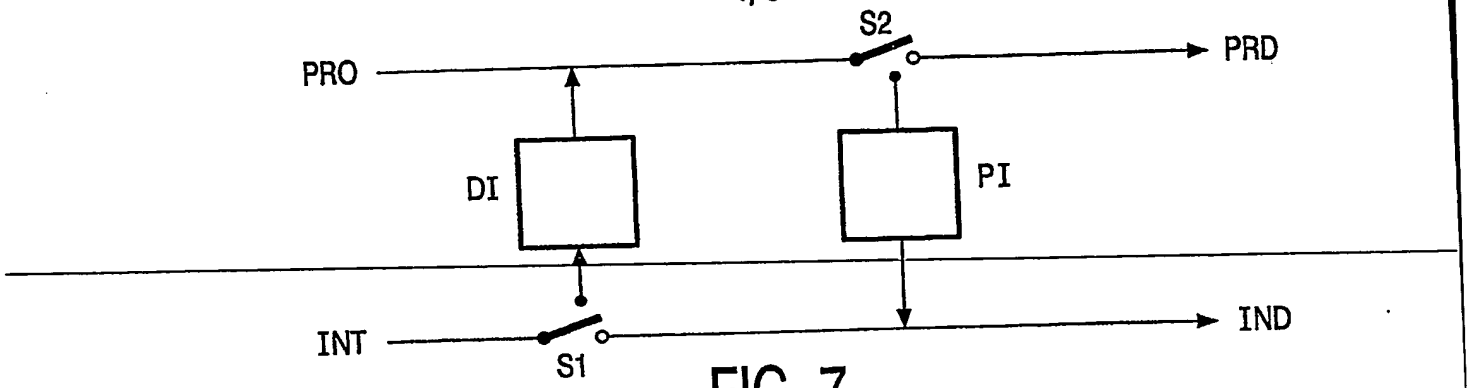

FIG. 7

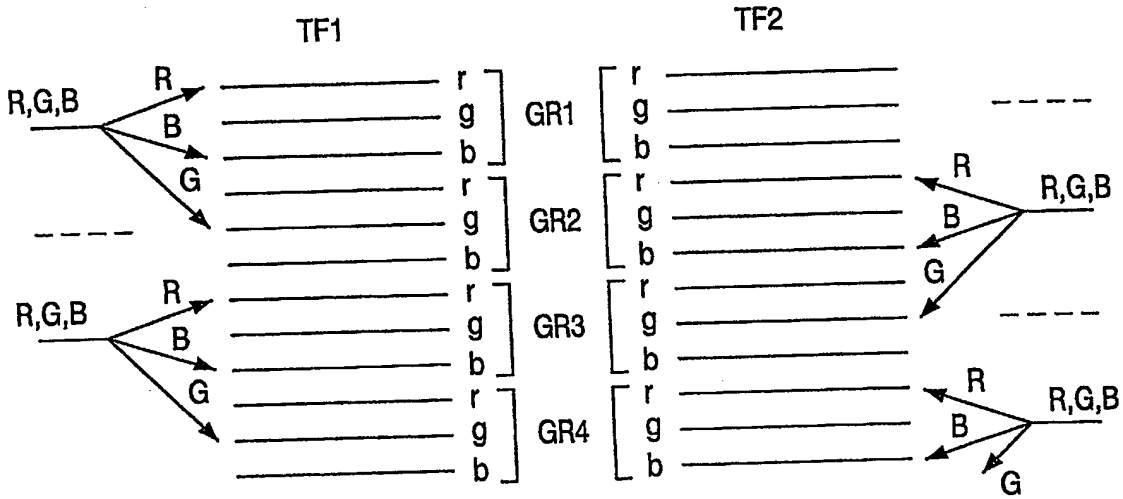

FIG. 8A

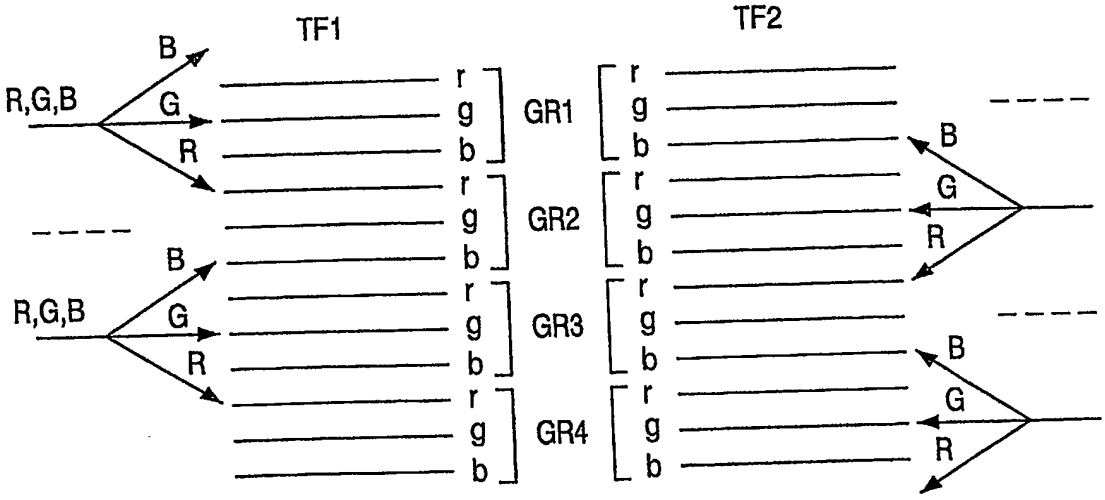

FIG. 8B

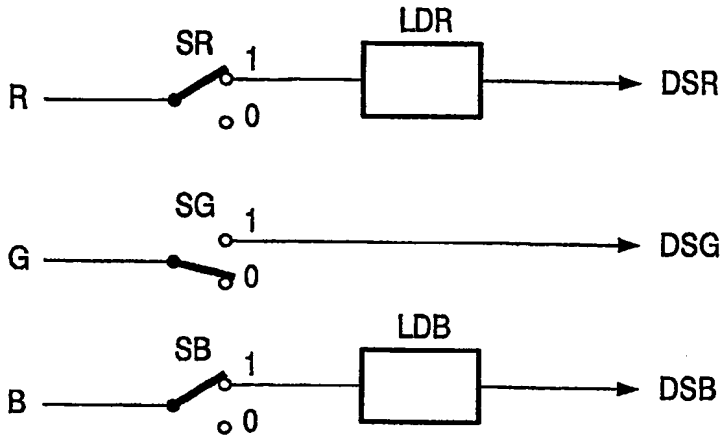

FIG. 9

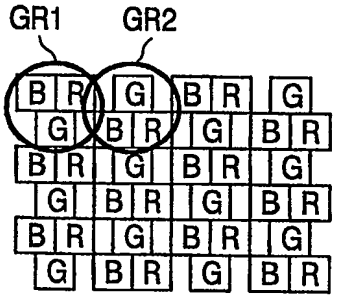

FIG. 10A

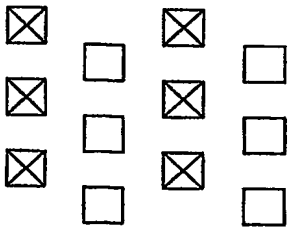

FIG. 10B

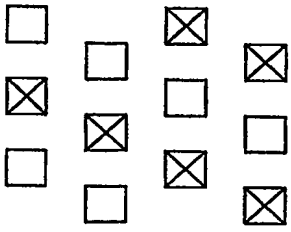

FIG. 10C

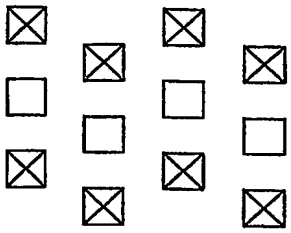

FIG. 10D

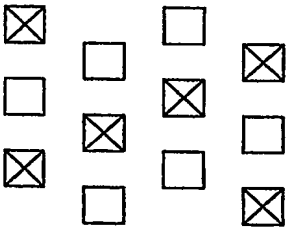

FIG. 10E